REMARKS

Claims 1, 3-8, 10-24 are pending in this application. Claims 1, 3, 4, 6, 8, 10, 11, and 13 are independent. Claims 19-24 are new.

Claim Rejection – 35 USC 102(b)

Claims 3 and 10 have been rejected under 35 U.S.C. 102(b) as being anticipated by JP 01-223586 ("Omichi"). Applicants respectfully traverse this rejection.

The invention of claim 3, in a preferred embodiment, is directed to a microcomputer having a built-in nonvolatile memory. A test program for testing the nonvolatile memory is received through a communication circuit under the control of a control program contained in a boot ROM. The test program is run using a RAM. Claim 10 is directed to an IC card packing a microcomputer.

The Office Action states that Omichi's ROM 4 (alternatively being a EEPROM) teaches the claimed nonvolatile memory and the claimed boot ROM, and that Omichi's RAM 5 teaches the claimed RAM. Applicants submit that Omichi's ROM does not teach both the claimed nonvolatile memory and boot ROM.

In the present invention, the boot ROM contains a control program for enabling receiving of the test program from an external check system upon receiving a test command issued by the external check system. The test program is for the nonvolatile memory of the microcomputer. In order to make this distinction clear, Applicants have amended claim 1 to indicate that the nonvolatile

memory, unlike a ROM, is "an at least partially erasable built-in nonvolatile memory." Applicants submit that Omichi's ROM 4 does not teach both a boot ROM comprising a control program for enabling receiving the test program for a nonvolatile memory and the at least partially erasable built-in nonvolatile memory that is the subject of the testing by the test program.

At least for this reason, Applicants submit that the rejection fails to teach each and every claimed element. Applicants respectfully request that the rejection be withdrawn.

Claim Rejection – 35 USC 103; Omichi, Lin

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omichi in view of U.S. Patent No. 5,818,848 ("Lin"). Applicants respectfully traverse this rejection.

The Office Action relies on Lin to make up for a deficiency of Omichi of failing to teach a plurality of microcomputers each having a built-in nonvolatile memory, and wherein the check system comprises a control computer connected to a plurality of external communication devices, for intensively controlling a check-up of the plurality of microcomputers each connected to respective external communication devices. (Office Action, pages 3-4).

Lin shows a mechanism including a test control processor 100 and a test board 101 for gang testing of integrated circuits. The test control processor may control the integrated circuits to execute tests in parallel, with the results of the

tests being stored in non-volatile memory on each integrated circuit. (with respect to Figures 1 and 2, paragraph bridging columns 4-5).

Applicants submit that even given the teachings of Omichi and Lin, either alone or in combination, they would not anticipate the claimed invention as a whole.

In the present invention, each boot ROM in the respective plurality of microcomputers has a control program for jobs of upon receiving a test command issued from the control program, receiving the test program for the nonvolatile memory from the check system.

In Lin, on the other hand, the test control program is provided to the integrated circuits under the control of the test control processor (Lin at column 5, lines 4-7). Lin does not disclose a plurality of microcomputers including a boot ROM having a control program for jobs including receiving the test program from the check system, e.g., test control processor.

Thus, Lin fails to make up for the deficiency of Omichi of failing to teach or suggest each microcomputer having both a boot ROM comprising a control program for jobs including receiving the test program for a nonvolatile memory and the at least partially erasable built-in nonvolatile memory.

Accordingly, Applicants submit that the rejection fails to establish *prima facie* obviousness. Applicants respectfully request that the rejection be withdrawn.

Claim Rejection – 35 USC 103; Omichi, Chan

Claims 1, 4, 6, 8, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omichi in view of U.S. Patent No. 5,029,168 ("Chan").

Claim 1, in a preferred embodiment, is directed to a microcomputer having a built-in nonvolatile memory including a communication circuit which is controlled by a control program contained in a boot ROM. Upon receiving a test command issued by an external check system, the control program enables receiving of a test program from the external check system by way of the communication circuit.

The Office Action states that Omichi fails to disclose "upon receiving a test command issued by the external check system, enabling said receiving of said test program from said external check system through said communication circuit," and instead relies on Chan to make up for the deficiency. The Office Action further states that, "Chan discloses handshaking wherein a host computer, or external check system, transmit a signal to a PC or UUT, thus indicating receiving a test command issued by the external check system, and if it is connected correctly, the PC or UUT transmits signal back to the host computer enabling the host computer to send out of software instructions, thus indicating enabling said receiving of said test program from said external check system through said communication circuit." Applicants disagree with the interpretation provided in the Office Action.

Claim 1 clearly recites "enabling said receiving". The term "said receiving" refers to the function recited in the claimed communication circuit of, "receiving a test program for a nonvolatile memory from an external check system." Thus, Applicants disagree that the preparation steps of a handshaking procedure anticipates the function of the boot ROM in conjunction with the communication circuit as recited in claim 1.

Similar arguments apply as well to independent claims 4, 6, 8, 11, and 13.

Furthermore, in order to clarify that the claimed boot ROM is not also the claimed built-in nonvolatile memory, independent claims 1, 4, 6, 8, and 11 have been amended to recite that the non-volatile memory that is the subject of the test program is "an at least partially erasable built-in nonvolatile memory." Applicants submit that Omichi's ROM does not teach both the claimed nonvolatile memory and boot ROM.

Similar arguments apply as well to independent claims 4, 6, 8, 11, and 13.

Accordingly, Applicants submit that the rejection fails to establish *prima facie* obviousness. Applicants respectfully request that the rejection be withdrawn.

Claim Rejection – 35 USC 103; Omichi, Chan, Lin

Claims 5, 7, 12, 14, 15, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omichi, Chan, and Lin. Applicants respectfully traverse this rejection.

The same arguments as in the above for claims 1, 4, 6, 11, and 13 apply as well to dependent claims 5, 7, 12, 14, 15, 17, and 18. Accordingly, Applicants respectfully request that the rejection be withdrawn.

New Claims

Claims 19-24 have been added. New claims 19-22 further define the function of "receiving" as comprising allocating an area on the RAM sufficient to receive the test program, which is based on the disclosure at page 24 of the present specification. Applicants submit that Omichi, Chan, and Lin, either alone or in combination, fail to teach or suggest at least the limitation expressed in new claims 19-22.

New claims 23 and 24 explicitly recite that the boot ROM is detached from the nonvolatile memory. Applicants submit that Omichi's ROM 4 does not teach or suggest the boot ROM, as recited in the claims, detached from a nonvolatile memory.

CONCLUSION

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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